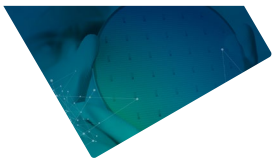
Aeneas

Engage in the digital future!

Article

Paris, 12 December 2023



Pilot Lines and Design Platform announced at Chips JU Launch event- Chips for Europe

There were big announcements and a large attendance at the Chips Joint Undertaking (JU) Launch Event in Brussels, 30 November to 1 December 2023. Over 800 people participated in person or online, demonstrating huge interest in the European semiconductor industry. Among the headlines: The Chips JU is launched. Calls for four new Pilot Lines covering critical strategic technologies are now open. And first calls for the virtual Design Platform will open in Q1 2024.

In his introduction, Jari Kinaret, Chips JU Executive Director, said "It is not just about chips". Geopolitics are driving the need for a more robust Electronic Components and Systems (ECS) value chain. And "a strong industry, a coherent approach, and synergies are vital for Europe's digital transformation". With its tripartite structure – European Commission (EC), Participating States, and Industry – the Chips JU has a unique leverage, able to support hundreds of projects, he added.

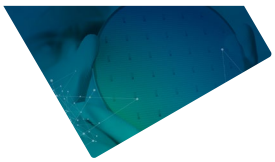
Pilot Lines, Design Platform, and support to elevate EU leadership

EU Commissioner for the Internal Market, Thierry Breton, spoke of Europe's ambitions to be an industry front-runner, with capabilities in advanced technologies as well as in existing strengths. He praised the world-beating 11 billion euros of investment in R&D through the Chips JU, and confirmed the creation of a European cloud-based design platform and four new pilot lines. These lines will bridge the gap from the lab to the fab in four critical and strategic technologies:

- extending Moore's law to the Angstrom area
- scaling down towards 7 nm in FD-SOI technology
- the integration of several heterogeneous technologies and advanced packaging
- next-generation wide-bandgap materials.

Access to the pilot lines and design platform will be facilitated by a network of European Competence Centres. In addition, the EC will facilitate access to capital (particularly for SMEs) through the Chips Fund, invest in competences and skills leading to 25,000 direct jobs, and increase the focus on quantum technologies.

Mr. Breton further announced the launch of the Industrial Alliance on Processors and Semiconductor technologies. He also welcomed the first meeting of the European Semiconductor Board on 30 November, as well as the 21 billion IPCEI on Microelectronics and Telecommunication Technologies launched earlier this year.



Access and timings

In later sessions, Yves Gigase, Head of Programmes Chips JU, and Anton Chichkov, Programme Officer Chips JU, explained that the Pilot Lines will be co-owned 50/50 by the Chips JU and national entities in EU Member States and/or the hosting organisation. The call process and consortia will be more complex than usual as they will cover equipment purchase, hosting, installation, and operation. The lines will be open to all, from SMEs to large companies, with training and links to verticals also being a potential part of their role. Calls are now open and will close on 29 February 2024, with selection due in Q1 2024 and operations may begin before end 2024.

Introducing the Design Platform, Marco Ceccarelli, Programme Officer DG CNECT, and Matthew Xuereb, Policy Officer DG CNECT, explained that in a "fabless world" design delivers high value and fast growth, but Europe's share of global revenues has dropped to 1-2%. The EU's Design Platform will be vendor neutral and provide access to EDA tools and IP libraries (proprietary and open source), as well as services, in a secure, interoperable, scalable, and flexible environment – with the goal of a faster, cheaper design process, particularly for SMEs.

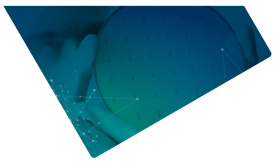
The platform will reduce barriers to entry e.g. cost and licensing, and facilitate access to the Pilot Lines for steps from prototyping to tape out. More widely, the platform should foster collaboration and enable training on EDA tools. Moving ahead, it will also support quantum technologies and integration of AI (including to address the shortage of skills in design).

The Competence Centres will be co-funded by the Chips JU and Member States and will focus strongly on SMEs and skills development, offering services for free or at low cost. First calls are expected in Q2 2024.

On finance, EC officials outlined how the European Innovation Council (EIC) Accelerator primarily supports early, smaller ventures with schemes for different TRLs; while InvestEU supports more mature enterprises. Info Days on the EIC Accelerator will be held in mid-January 2024.

Securing European lead in quantum technologies

On quantum, Gustav Kalbe, acting Director DG CNECT, described advances in quantum computing and sensing in areas from healthcare to communications. The EU has a world-leading and vibrant start-up industry, and it sees the link to the Chips JU and Pilot Lines as essential to scale up and attract investment. The pilot lines should be valuable in evaluating technology options, especially whether building on existing photonic or semiconductor technologies is a feasible route to secure early market advantage.



SRIA and first calls

Later, Patrick Cogez, Technical Director of AENEAS, outlined an amendment of the ECS SRIA 2023 (Strategic Research & Innovation Agenda) related to the Chips JU initiatives, including linkage with the Pilot Lines and Design Platform. Sustainability, photonics, quantum sensing and AI are also now integrated in the SRIA, with ECS seen as an enabler of trustable, responsible AI. The ECS SRIA amendment is a basis of the Pilot Lines Call and their amended Work Programme 2023.

The following session introduced the 'non-initiative' calls which will be launched on 6 February 2024 and close on 14 May. They should cover Advanced Packaging for MM Wave and sub-THz applications, AI assisted methods and tools for ECS engineering efficiency, vehicle of the future, and sustainable and green manufacturing (details to be confirmed on the Chips JU portal here).

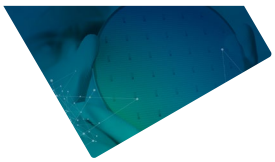
Speakers and panelists discuss strategic issues

Nikolai Setzer, CEO, Continental AG; Jochen Hanebeck, CEO Infineon Technologies; Lucilla Sioli, Director for "Artificial Intelligence and Digital Industry" EC DG CNECT; and Jean-Luc di Paola-Galloni, Chair Chips JU Private Members Board, gave speeches on topics from EU strategy to the role of the Industry Associations (AENEAS, EPoSS, Inside) in the Chips JU.

In his speech, Jaime Martorell, Special Commissioner for Microelectronics and Semiconductors, Spain, stressed that Europe cannot 'go for it alone', but it can build on existing strengths and create more resilient supply chains. He also talked about diversification across Europe's regions, mentioning Spain's 12-billion-euro investment in semiconductor design and production capacities.

The panel discussions covered numerous themes including: targeting funding to get the biggest impact; the EU regulatory environment, skills and jobs with 'purpose' for young people; sustainability and decarbonisation, new materials and processes, and bringing back packaging capabilities to the EU. Sovereignty, autonomy, and security were also seen as key, as were partnerships with like-minded partners such as Canada and South Korea (in Horizon Europe and Eureka).

Finally, many called for the next Commission to continue prioritising the ambitions and initiatives set out in the Chips Act. Meanwhile, in the words of Commissioner Breton: Europe has a very ambitious plan. It must now implement it and do so with speed.



About AENEAS:

AENEAS is an Industry Association, established in 2006. The purpose of the association is to promote Research, Development and Innovation (RD&I) to strengthen the competitiveness of European industry across the complete Electronics Components and Systems (ECS) value chain. AENEAS provides unparalleled networking opportunities, policy influence & supported access to funding to all types of RD&I participants in the field of micro and nanoelectronics-enabled components and systems, and its applications. Partner in KDT JU and the newly launched Chips JU, AENEAS is also operating the Eureka-funded Clusters Xecs, PENTA, and EURIPIDES².