Aeneas

Engage in the digital future!

Article

Paris, 19 May 2022

EC Staff Working Document gives added details on EU Chips Act

On 12th May 2022, the European Commission (EC) published a 'Staff Working Document' (SWD) on the proposed European Chips Act package. This document gives in-depth background on the rationale behind the Act. It also describes the implementation, governance and funding of the Act's three pillars: Chips for Europe, Security of Supply and Monitoring & Crisis Response.

The EC introduced the European Chips Act proposals on 8th February 2022. These were announced earlier than originally planned due to the ongoing impact of global chip shortages. However, the package's rapid introduction did not allow time for the normal EU Impact Assessment. The SWD compensates for this with an extensive analysis of all aspects of the proposals.

In opening, the SWD explains the aims of the Act, the global semiconductor landscape, Europe's current market position, and technology trends and opportunities for European industry. It stresses the need for Europe to convert "its excellent research" into industrial innovation. And it calls for greater end-user company participation in the semiconductor ecosystem and a focus on serving key industry sector needs.

The SWD then discusses the specifics of the Chips Act, providing a detailed discussion of each Pillar.

Pillar 1 – Chips for Europe Initiative and Chips JU

To quote the SWD: *"Pillar 1 of the Chips Act, the Chips for Europe Initiative, will create an ecosystem to build up coordinated R&D efforts and technological capacity at scale throughout the Union." "It aims to close the gap from lab to fab … by leveraging European strengths and reinforcing technology capacities."*
The document further adds: *"That will only work through a collective effort by all stakeholders: EU and Member States across the Union; industrial actors across the full value chain; researchers and RTOs."*

• The Chips JU – R&I and capacity building

In the light of these goals, the SWD explains how the Chips Act would transform the existing Key Digital Technologies (KDT) Joint Undertaking (JU) into the Chips JU via an amendment to the Single Basic Act (SBA). (The SBA established 9 European JUs under Horizon Europe in November 2021).

Specifically, *"…. the SBA amendment makes relatively minor changes to prepare the KDT JU for the implementation of the Chips for Europe Initiative, to adjust its governance accordingly, and to introduce capacity building activities."*

Moreover, *"Apart from the introduction of capacity building activities for the four components of the Chips for Europe Initiative, coverage of the Chips JU would not be substantially different from that of the KDT JU."* The four components referred to are:

- design capacities for integrated semiconductor technologies;
- pilot lines for preparing innovative production, and testing and experimentation facilities;
- advanced technology and engineering capacities for quantum chips; and
- a network of competence centres and skills development.

(The fifth component, which would not be implemented within the Chips JU, is the Chips Fund*, "… a dedicated semiconductor investment facility.*")

Further, the SWD says*: "It should be noted that many activities that would be considered research and innovation activities on the four components of the Chips for Europe Initiative are currently supported by the KDT JU and previously by the ECSEL JU. Examples are research and innovation activities on pilot lines supported by ECSEL … and the development of open-source RISC-V building blocks under KDT Work Programme 2021."*

In practice, this means that: *"… the Chips JU would implement activities under the original KDT JU (also known as 'non-Initiative' activities) and activities under the Chips for Europe Initiative. The latter activities could be broken down in research & innovation activities and in capacity building activities. The original KDT activities are research & innovation activities. All research & innovation activities will be based on the Strategic Research and Innovation Agenda prepared by the industry associations. Horizon Europe would be the funding source for research & innovation activities, whereas the Digital Europe Programme would fund capacity building activities."*

• ECIC – new consortium mechanism

Also under Pillar 1, the SWD describes the new 'European Chips Infrastructure Consortium (ECIC)' mechanism. It explains that: *"The main aim of an ECIC is to encourage effective and structural collaboration between legal entities, including Research and Technology Organizations and Member States."*

In particular, the ECIC mechanism would facilitate the implementation of parts of the Chips for Europe Initiative such as the set-up of the new pilot lines. *"For this, the Chips JU would launch a call for expression of interest, calling for an ECIC to implement the specific activity."*

"The procedure and the details for the expression of interest of an activity to be implemented by an ECIC … would have to be decided in the Work Programme of the Chips JU as an implementing body of the Initiative."

And among other advantages, the ECIC mechanism would allow a combination of *"… funding from the Member States, the Union and from the private sector, including throughout a longer timeframe than the current Multiannual Financial Framework (MFF)."*

- ## Virtual design platform

A key part of the Chips for Europe Initiative is the creation of a virtual design platform and of pilot lines that are open for research, testing, experimentation and validation of new device concepts. The SWD sets out how these facilities would function and what they would offer.

It adds that: *"This would all be networked together and made widely available in Europe, creating a large capability with potential innovations in all relevant technologies such as FDSOI, FinFET, heterogeneous integration, and silicon photonics, but also others for particular applications".*

Expanding on the nature of the design platform, the SWD says the Act would enable the creation of: *"A (virtual) design platform accessible across the EU offering Electronic Design Automation (EDA) tools, IP libraries (created and combined by RTOs and participants across the EU) and integrating and standardising libraries from existing pilot lines".* This platform would be continuously upgraded and *"… will stimulate a wide cooperation of users' communities with design houses, IP and tool suppliers, designers and RTOs, and cater for the design of novel components and systems for multiple applications such as low energy, security, system integration and 3D assembly".*

In this way, the Chips for Europe Initiative *"… will provide the R&D community, RTOs, suppliers of technology services, industry, SMEs and start-ups across Europe with ready access to the most advanced technology and design infrastructure."*

- ## Pilot lines

Concerning pilot lines, the SWD foresees initially harnessing the existing facilities to deliver results for production around 2024-2026. *"New pilot lines will then be added to this infrastructure to address the most advanced technologies, aiming to fill the gaps in Europe's technological capability and reach the 2030 ambition of being at the leading edge for advanced production capabilities."*

Further, the SWD notes that: *"There are currently at least 16 existing pilot lines in 10 Member States." "These were for the most part developed under partnership, the ECSEL JU and the Photonics21 public-private partnership, and some have already demonstrated technologies from EUV to FinFET and FD-SOI to heterogeneous integration and graphene as well as photonic integrated circuits."*

For new pilot lines, the SWD says: *"These will be developed as research pilot lines to address specific technology challenges, including test and validation. They will have different characteristics in view of satisfying the user requirements, and maximise the successful transfer of results into the industrial environment. The relative involvement of research organisations and industry will depend on the level of technological maturity addressed."*

Discussing the benefits of the technology infrastructure foreseen in the Act, the SWD remarks: *"For the pilot lines, research and innovation activities would develop – for example – technologies to achieve transistor sizes below 2 nm, novel materials, as well as heterogeneous and 3D integration of different materials. Such R&I activities could be performed together with ongoing research on advanced materials, thereby contributing to HE Cluster 4 objectives."*

Furthermore: *"Although these pilot lines address different technologies, operating them under a single structure will maximise the synergies between them and bring benefits."*

- Synergies between design platform and pilot lines

Indeed, the SWD stresses that synergies are key to the Chips Initiative as a whole: "… the design platform and pilot lines should operate in a synergistic way". And it describes how the EC intends this to happen.

"… in each Member State design houses and competence centres will be set up to provide access to the tools and libraries and to coach people in how to use the new infrastructure. Linking these through a network of competence centres will ensure sharing of information, and local access for users to expertise, to the design platform with its tools and libraries, and to the use of the pilot lines on a pan-European level."

Further, it says that the technology infrastructure, *"… through the involvement of competence centres and the EDIHs [European Digital Innovation Hubs], will act as an aggregator of customer requests (in particular from SMEs and start-ups) and bundle them into runs in pilot lines or commercial fabs. The direct benefits will be (i) substantially lower costs of accessing the technologies being piloted; and (ii) an acceleration of the innovation cycle with seamless design, prototyping and manufacturing processes resulting in faster development of products."*

Pillar 2: Security of Supply – 'first of a kind' facilities criteria and operation

Under Pillar 2, the SWD details the need to increase production capacity via 'first of a kind facilities' – either an 'Integrated Production Facility' or an 'Open EU Foundry'. It explains the procedures to obtain 'first of a kind' recognition and authorisation for State aid, plus fast-tracking of planning and permissions. The document further notes that the approach proposed for assessing State aid for 'first-of-a-kind facilities' is "… *complementary to the framework of Important Projects of Common European Interest (IPCEI) … which is intended to support multi-country R&I projects up to first industrial deployment in areas of common interest, thus supporting a different stage of the innovation cycle.*"

There is also a discussion of how these facilities would fit within the envisaged pan-European ecosystem. Among other things, the Integrated Production Facilities and Open EU Foundries would receive priority access to the pilot lines set up under the Chips for Europe Initiative.

- Pillar 2 timeline

The SWD stresses the urgency: *"Investments now will allow increasing production capacity in the EU as of 2025-26 in more mature nodes. And investments now in leading-edge nodes, starting with advanced pilot lines, are needed to develop knowledge and skills and be able to translate such investments in new production capabilities at 2 nm or below around 2028-2030 in Europe."*

Pillar 3: Monitoring and Crisis Response – role of Member States and industry

Pillar 3 of the Chips Act aims to establish mechanisms that will allow the EU and Member States to understand the dynamics of global semiconductor markets and thereby to anticipate and avoid future shortages. Here, the SWD provides a comprehensive overview of how the monitoring and crisis response will be governed and implemented.

It stresses that: *"The proposed monitoring and crisis response mechanism … introduces crisis response measures only where these are necessary, appropriate and proportionate in order to ensure supply to critical sectors and in close dialogue with Member States and experts through the European Semiconductor Board."*

Governance – role of The European Semiconductor Board (ESB)

The ESB is an important part of the new governance structures under the proposed Chips Act. It would consist of representatives from the Member States and be chaired by the Commission. In the SWD, it is described as the "overarching governance structure for the three pillars of activity" and as an "advisory board".

Within the Chips JU, the ESB would provide advice to the Public Authorities Board (PAB). It would also act as an advisory body to the Integrated Production Facilities and Open EU Foundries. Plus, it would serve as the coordination mechanism and be consulted on monitoring and crisis response measures in Pillar 3.

The SWD further mentions that the ESB may invite *"organisations representing the interests of the semiconductor industry to participate".* For example, members of the Industrial Alliance on Processors and Semiconductor Technologies could be invited to advise on the Chips JU work programme.

Chips JU Governing Board

While the ESB would have an advisory role to the PAB in the Chips JU, there would be no change to the JU's Governing Board. *"The Governing Board, which would still consist of representatives of participating states, private members, and the Commission, would continue being the main decision-making body of the Joint Undertaking. The GB has the overall responsibility for the strategic orientation and operations of the Joint Undertaking as well as their coherence with relevant Union objectives and policies. In a nutshell, it supervises the implementation of the Joint Undertaking's activities and adopts its work programmes."*

Budget for Chips JU

The SWD provides an overview of the public financial contribution to activities within the Chips Act, including a detailed breakdown of EU funding for the Chips for Europe Initiative. It states: *"Article 128 of the proposed amendment to the SBA, as regards the Chips JU, indicates that the proposed Union financial contribution 'shall be up* ***to EUR 4.175 billion'****."* Some of this total will be earmarked for capacity building, with the rest going to original KDT activities and R&I activities within the scope of the Chips for Europe Initiative.

In the words of the SWD: *"Capacity building activities under the Chips JU would be funded via the Digital Europe Programme and would be limited to the four components of the Chips for Europe Initiative; they would not cover the full scope of the current KDT JU."* The table below shows the figures involved (in millions of Euros).

	Chips for Europe Initiative	**Non-initiative**	**Total**
Research & Innovation (Horizon Europe)	*1.350*	*1.300*	*2.650*
Capacity building (Digital Europe)	*1.525*	*n.a.*	*1.525*
Total	*2.875*	*1.300*	*4.175*

Measuring success

Concluding, the SWD says that success of the EU Chips Act will be measured against the objective of the 2030 Digital Compass, targeting that Europe will deliver 20% of world semiconductors production by that date. It also seeks tangible progress on strengthening EU research and technology leadership; addressing the skills shortage; reinforcing Europe's capacity in design, wafer manufacturing and packaging; and developing an in-depth understanding of global semiconductor supply chain so that the EU can take appropriate measures when necessary.